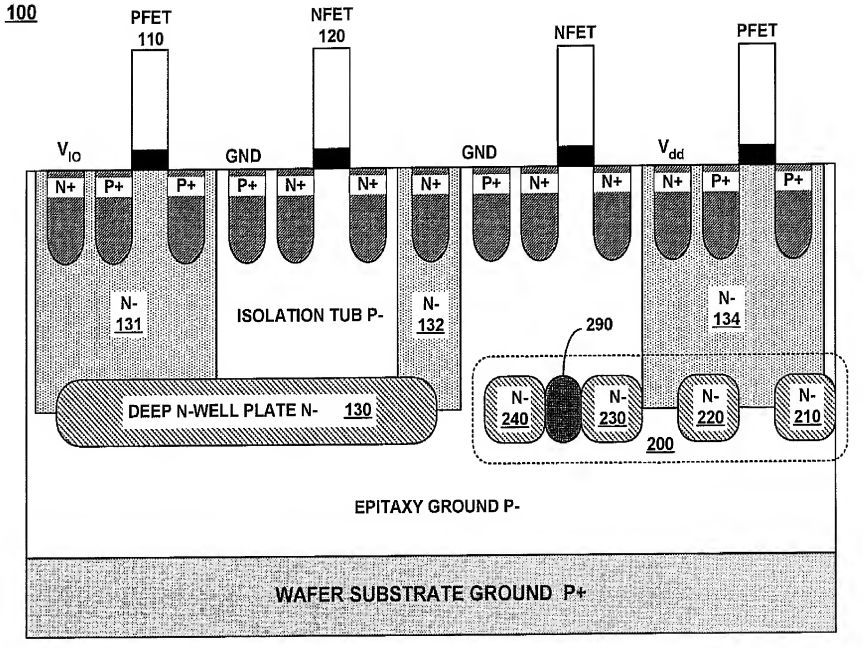
100
PFET
110
NFET
120
NFET
PFET
V_{IO}
GND
GND
V_{dd}
N+
P+
P+
P+
N+
N+
N+
N+
P+
N+
N+
N+
P+
P+
N-
131
ISOLATION TUB P-
N-
132
290
N-
134
DEEP N-WELL PLATE N-
130
N-
240
N-
230
N-
220
N-
210
200
EPITAXY GROUND P-
WAFER SUBSTRATE GROUND P+

FIGURE 1

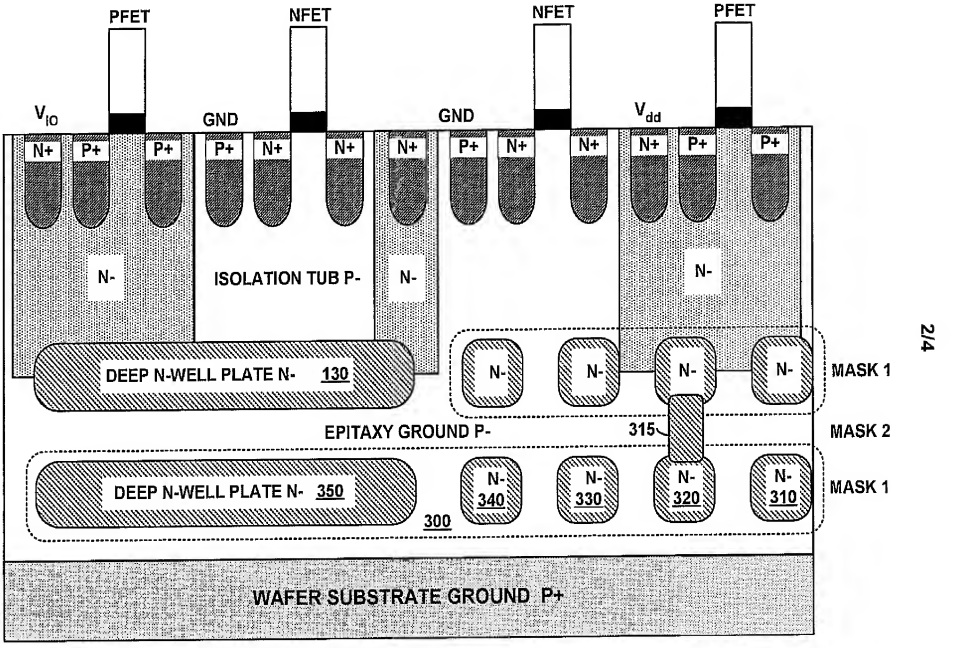
PFET
NFET
NFET
PFET
V_{IO}
GND
GND
V_{dd}
N+
P+
N-
ISOLATION TUB P-
DEEP N-WELL PLATE N- 130
MASK 1
EPITAXY GROUND P-
315
MASK 2
DEEP N-WELL PLATE N- 350
340
330
320
310
MASK 1
300
WAFER SUBSTRATE GROUND P+

FIGURE 2A

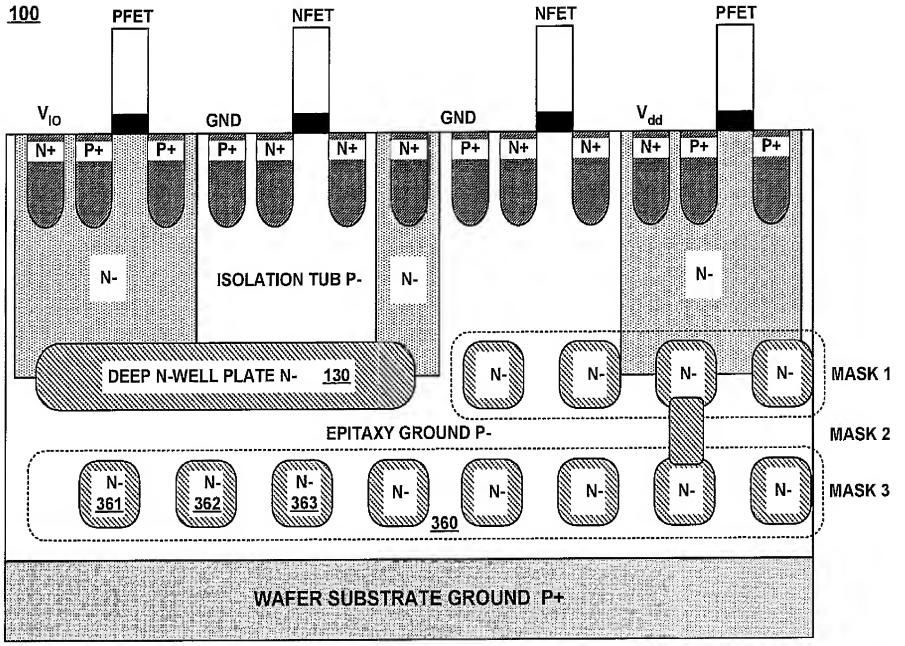
100
PFET
NFET
NFET
PFET
V_{IO}
GND
GND
V_{dd}
N+
P+
N-
ISOLATION TUB P-
DEEP N-WELL PLATE N- 130
EPITAXY GROUND P-
MASK 1
MASK 2
MASK 3
N- 361
N- 362
N- 363
360
WAFER SUBSTRATE GROUND P+

FIGURE 2B

400

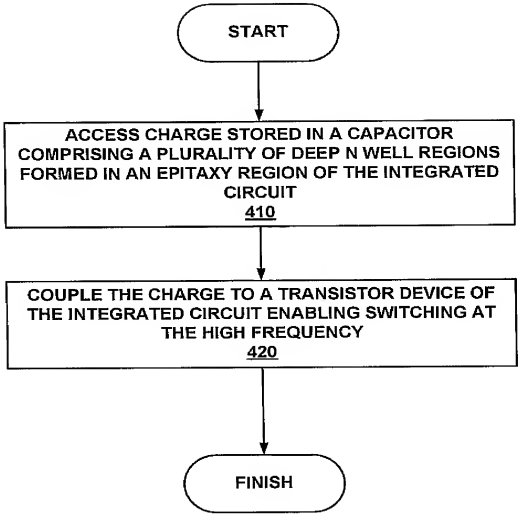
START
ACCESS CHARGE STORED IN A CAPACITOR COMPRISING A PLURALITY OF DEEP N WELL REGIONS FORMED IN AN EPITAXY REGION OF THE INTEGRATED CIRCUIT
410
COUPLE THE CHARGE TO A TRANSISTOR DEVICE OF THE INTEGRATED CIRCUIT ENABLING SWITCHING AT THE HIGH FREQUENCY
420
FINISH

FIGURE 3